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09/527,497	03/16/2000	Sunil C. Shah	001340,zp006q	2379

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Darren J Milliken
Blakely Sokoloff Taylor & Zafman LLp
12400 Wilshire Boulevard 7th Floor
Los Angeles, CA 90025

EXAMINER	
THOMSON, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2123	5

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/527,497	SHAH, SUNIL C.	
	Examiner	Art Unit	
	William D. Thomson	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 have been submitted for examination.

2. Claims 1-42 have been examined and rejected. THIS ACTION IS MADE FINAL.

Drawings

3. Applicant filed formal drawings for the instant specification on November 25, 2003. These drawings are acceptable for examination purposes. The drawings have not been reviewed by the draftsman since there appears to be an outstanding objection regarding figure 1.

4. In response to the non-response provided by the Applicant regarding this issue, Examiner now points to the prior art Shah et al. (959) shown as Fig. 3, which published March 9, 1999, more than a year prior to the filing of the instant invention. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See M.P.E.P § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

PRIOR ART REJECTIONS

5. Claims have been afforded their broadest reasonable interpretation. Applicant's language directed to diagram and ordering of blocks has been interpreted as the standard features provided in windows based GUI SPICE simulators that allow the user to reorder the circuits during simulations, add circuit layouts and simulate the changes in a graphical environment. The retro events and backtracking events to reorder and improve the simulation blocks of the applied art are equivalent to the recitations of ordering the blocks in the block diagram structure.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazmierski et al. (217) in view of Shah et al. (959) and Martin et al. (345), individually.

Taking claim 1, for example Kazmierski et al. (217) teaches:

A method for simulation modeling where the simulation model includes individual blocks in a block diagram structure wherein each of the individual blocks include equation sets of a physical model, comprising the steps of: (see Abstract, Figures 1-10, Summary of the Invention, col. 4, lines 34 et seq.)

configuring said blocks in a block diagram structure; (col. 4, lines 34 et seq., figures 1-10)

utilizing commercial simulation software to solve said equation sets of said blocks; (col. 6, lines 33-40, SPICE)

ordering said blocks in said block diagram structure to allow for waveform relaxation of sets of variables of said blocks; and (col. 5, lines 5 et seq,)

performing waveform relaxation of said sets of variables of said blocks. (col. 4, lines 34 et seq.)

As to claim 2, the method of claim 1, wherein said step of ordering said blocks in said block diagram structure includes decomposing said block diagram into subsystems is taught within Kazmierski et al. (217) at col. 5, lines 5 et seq.

As to claim 3, the method of claim 1, wherein said step of ordering said blocks in said block diagram structure includes identifying said sets of variables of said blocks is taught within Kazmierski et al. (217) at col. 5, lines 5 et seq.

As to claim 4, the method of claim 1, wherein said step of ordering said blocks in said block diagram structure includes adding a low fidelity model of one of said blocks is taught within Kazmierski et al. (217) at col. 5, lines 5 et seq.

As to claim 5, the method of claim 4, wherein said sub-step of adding said low fidelity model of one of said blocks includes deriving an error signal from an output of said one of said blocks and an output of said low fidelity model is taught within Kazmierski et al. (217) at col. 5, lines 5 et seq.

As to claim 6, the method of claim 5, wherein said step of ordering said blocks in said block diagram structure includes accelerating convergence of said simulation model by processing said error signal is taught within Kazmierski et al. (217) at col. 6, lines 58 et seq.

As to claim 7, the method of claim 1, wherein said step of performing waveform relaxation includes deriving a sparse interconnect matrix is taught within Kazmierski et al. (217) at col. 6, lines 58 et seq.

As to claim 8, the method of claim 7, wherein said step of performing waveform relaxation includes weakly-coupling said equation sets is taught within Kazmierski et al. (217) at col. 5, lines 65 et seq.

As to claim 9, the method of claim 8, wherein said step of utilizing said commercial simulation software includes running said commercial simulation software on a plurality of data processors is taught within Kazmierski et al. (217) at col. 6, lines 34 et seq.

As to claim 10, the method of claim 9, wherein said step of running said commercial software on said plurality of data processors includes waiting until each of said commercial simulation software has completed calculations before transmitting interprocessor communications data (IPC and API) is taught within Kazmierski et al. (217) at col. 7, lines 8 et seq., and col. 9, lines 4 et seq.

As to claim 11, the method of claim 1, wherein said equation sets change in subsequent iterations of said simulation model is taught within Kazmierski et al. (217) at col. 6, lines 58 et seq.

As to claim 12, the method of claim 11, wherein said equation sets increase in fidelity in subsequent iterations of said simulation model is taught within Kazmierski et al. (217) at col. 6, lines 58 et seq.

As to claim 13, the method of claim 1, wherein said step of performing waveform relaxation utilizes Gauss-Jacobi methods is taught within Kazmierski et al. (217) at col. 8, lines 37-44.

As to claim 14, the method of claim 1, wherein said step of performing waveform relaxation utilizes Gauss-Seidel methods is taught within Kazmierski et al. (217) at col. 8, lines 37-44.

However, Kazmierski et al. (217) is directed to designing circuitry and is not specific to the use of specifically designing a controller and where the controller controls a system for manufacturing, per Applicant's amendments.

Whereas both Shah et al. (959) is specific to using the methodology of Kazmierski et al. (217) in the design of a controller that that controls a system for

manufacturing. One of ordinary skill level at the time of the invention would have modified the teachings of Kazmierski et al. (217) with the teachings of Shah et al. (959) since; Kazmierski et al. (217) was directed to designing and implementing circuitry using waveform relaxations techniques and control circuitry is circuitry. Designing circuitry includes designing control circuitry, since all controls of this nature are circuits and Kazmierski et al. (217) uses a circuit as an exemplary teaching of using this method to improve the design process. Further, Shah et (959) is specific to teaching the use of waveform relaxation in designing the controller for a manufacturing process. One of ordinary skill level at the time of the invention would have necessarily knowingly modified the teachings of Shah et al. (959), which teaches the use of waveform relaxation but did not go into the level of detail as expounded upon by Kazmierski et al. (217) of the particulars of the waveform relaxation methodology. Kazmierski et al. expressly teaches designing circuitry with an extensive teaching of waveform relaxation methodology and Shah et al. (217) expressly teaches using waveform relaxation in the design of a controller for controlling manufacturing. Designers in the systems for control circuitry would have knowing of either teaching of Kazmierski et al. (217) would have implemented this in controls as taught in both Shah et al. (959) and Martin (345), at the time of the instant invention. Though Martin does not expressly use the waveform relaxation method, one of ordinary skill level at the time of the invention would have looked for a steady state modeling system that provides the methods as taught in Kazmierski et al. (217) to control their plant system. The method as used in Martin et al. (345) provides an equivalent solution, though not as eloquent as the methodology as

taught in Kazmierski et al. That person of ordinary skill level at the time of the invention would have necessarily modified Martin et al. with Kazmierski et al. (217) to yield the claimed invention since the result would be using the mathematical methodology of Kazmierski et al. (217) to generate the steady state model for the controlling circuitry as taught in Martin et al.(345) for the process plant control.

Claims 15-42 is rejected based on the same reasoning as claim 1-14, *supra*. Kazmierski et al. (217) in view of Shah (959) and Martin (345), individually.

CONCLUSION

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 C.F.R. 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William D. Thomson whose telephone number is 703-305-0022. The examiner can normally be reached on 8:30-3:30 Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William Thomson
Primary Examiner
A.U. 2123